

9. ~~12.~~ (Amended once) A memory module comprising:  
a first memory device;  
a second memory device stacked on the first memory device; and  
a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus;  
wherein the module is fabricated on a circuit board and further comprises a connector attached to the circuit board and adapted to couple the module to the bus.

10. ~~11.~~ (Amended once) A memory module comprising:  
a first memory device;  
a second memory device stacked on the first memory device; and  
a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus;  
wherein the memory module is adapted to receive a signal from the bus and to redrive the signal to another memory module.

11. ~~15.~~ (Amended once) A memory module according to claim ~~14~~ <sup>10</sup> wherein the memory module is adapted to receive a plurality of signals from the bus and to redrive the plurality of signals to another memory module.

12. ~~16.~~ (Amended once) A memory module comprising:  
a first memory device;  
a second memory device stacked on the first memory device; and  
a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus;  
wherein the buffer is adapted to receive a signal from the bus and to redrive the signal to another memory module.

17. (Amended once) A memory system comprising:  
a bus;  
a stack of memory devices; and  
a buffer coupled between the stack of memory devices and the memory bus, wherein the stack of memory devices is not stacked on the buffer.

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13. (Amended twice) A memory system comprising:

a bus;  
a stack of memory devices;  
a buffer coupled between the stack of memory devices and the bus;  
a second stack of memory devices; and  
a second buffer coupled between the second stack of memory devices and the bus;  
wherein the stacks of memory devices are not stacked on the buffers.

14.  
14. (Amended twice) A memory system comprising:

a bus;  
a stack of memory devices;  
a first buffer coupled between the stack of memory devices and the bus;  
a second stack of memory devices; and  
a second buffer coupled between the second stack of memory devices and the first  
buffer.

Please add the following new claims:

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24. (New) A memory system comprising:

a bus;  
a plurality of stacks of memory devices; and  
a buffer coupled between the plurality of stacks of memory devices and the bus.

25. (New) A memory system according to claim 24 further comprising:

a second plurality of stacks of memory devices; and  
a second buffer coupled between the second plurality of stacks of memory devices  
and the bus.

26. (New) A memory system according to claim 24 further comprising:

a second plurality of stacks of memory devices; and  
a second buffer coupled between the second plurality of stacks of memory devices  
and the first buffer.

27. (New) A memory system according to claim 24 wherein the buffer is adapted to receive a signal from the bus and redrive the signal to another buffer.

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28. (New) A memory module comprising:  
a circuit board;  
a first stack of memory devices mounted on the circuit board;  
a second stack of memory device mounted on the circuit board; and  
a buffer mounted on the circuit board and coupled to the first and second stacks of memory devices.

23.  
29. (New) A memory module according to claim 28 wherein the buffer is adapted to redrive signals.

24.  
30. (New) A memory module according to claim 28 further comprising:  
a third stack of memory devices mounted on the circuit board;  
a fourth stack of memory devices mounted on the circuit board; and  
a second buffer mounted on the circuit board and coupled to the third and fourth stacks of memory devices.

25.  
31. (New) A memory module according to claim 30 wherein the first buffer is adapted to redrive signals to another module.

26.  
32. (New) A memory module according to claim 30 wherein the first buffer is adapted to redrive signals to the second buffer.